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A LOW POWER, LOW DEAD ZONE PHASE FREQUENCY DETECTOR IN 180NM CMOS TECHNOLOGY FOR WIRELESS COMMUNICATION APPLICATION

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Abstract- This paper proposes a phase frequency detector designed in 0.18um CMOS Technology with 1.8V supply voltage. Three PFD architectures are simulated to get low dead zone and low power consumption. The DEC-PFD can avoid Up and DOWN signals from rising to high at the same time and thus solve current mismatch problem with 10-ps dead-zone in the phase detection. The circuit is simulated in Cadence Virtuoso analog design environment and the dead zone and current consumption is found to be 10 pS and 132.6 uA respectively. The circuit can be used in the application on high speed and low power phase locked loop circuit.
Keywords- Dead Zone, PFD, DEC, PLL, Power Consumption, sensitivity,

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Introduction

Phase locked loops (PLLs) are widely used in microprocessors and digital systems for clock generation and as a frequency synthesizer in communication systems for clock extraction and generation of a low phase noise local oscillator. In a PLL, PFD is used in measuring the frequency and phase difference between two input signals, i.e. the reference signal and the voltage controlled oscillator (VCO) output signal [1]. As shown in Fig.1, PFD detects the phase difference between the reference signal (EXT) and the VCO output Signal (INT). Output signals of the PFD are then produced as Up and DOWN pulses according to the phase difference between the two signals [1]. The output value of PFD will influence the output voltage of charge pump (CP) for VCO to tune according to that voltage, because the output voltage of charge pump (CP) is used to control the output frequency of VCO [2]. If a PFD can detect the smallest phase difference of output signal and reference signal of VCO, the PFD will have the best sensitivity. The best case for the smallest phase to detect is zero. However, the delay time of logic components and reset time of feedback path of flip-flop will cause a PFD to detect phase and frequency with distortion.

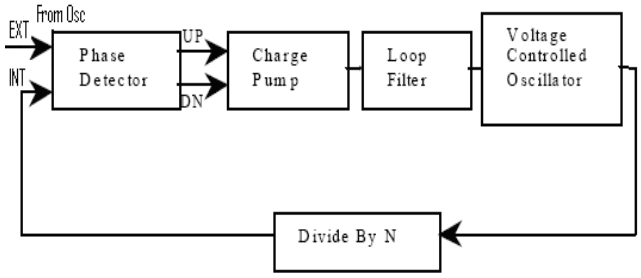

Fig. 1 - PLL Architecture

This is the main issue in the design of a PFD [3]. When delay time and reset time are large, a PFD cannot detect small phase error. The undetectable small phase range is called the dead zone. The size of the dead-zone will influence the effective sensitivity of a PFD. The aim of the design is to reduce PFD dead-zone value

and to achieve a low power consumption rate. The sensitivity of circuit is inversely proportional to the value of dead-zone [4].

PFD Architecture

We have compared three architectures the main aim was to minimize the reset path delay so that dead zone can be minimized and in the process by eliminating the components eliminating the components can bring down the power consumption. Traditional PFD, Modified PFD in which the reset path flip flop was omitted, Double edge checking PFD (DEC-PFD) which was designed by detecting the raising and falling edge of the input signals.

Traditional PFD Architecture

The design consists of two D flip-flops and a NOR gate in the reset path to reset both the flipflop when both outputs go high at the same time Fig.2 shows the block diagram of the architecture.

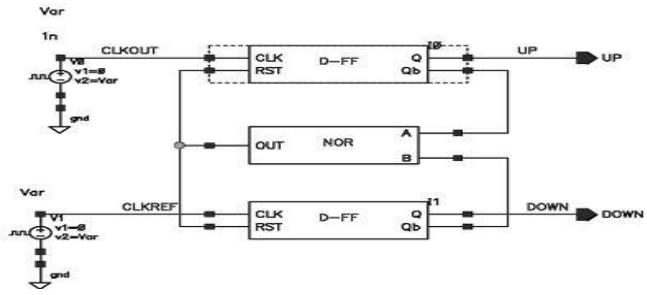

Fig. 2- Block Diagram of the Architecture

Due to this reset path this design suffer large dead zone.Fig.3 shows the schematic design of the D flip-flop for Traditional PFD.

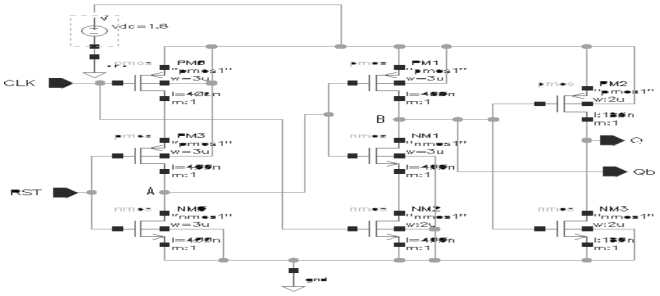

Fig. 3- Schematic design of the D flip-flop.

When CLK (CLOCK) and RST (RESET) are low, node A through pmos transistors PM0 and PM3 will be connected to VDD.At the raising edge CLK, node B will be connected to ground through nmos transistor NM1 and NM2. Since node A is connected to VDD that will turn off pmos transistor PM1 keeping node B from charging high. As RST signal charges up, node A will be connected to the ground through nmos transistor NM0, which will lead to pull up node B and it will become high due to switching pmos transistor PM1 on. Transistor PM3 job is to prevent a short circuit in the PM0, PM3 and NM0 path. When CLK is low and RST is high a large current will low this path so PM3 is placed there to prevent this current and lower the power consumption of the D flip flop[5].

Since we are getting flipped value of Q, an inverter has been added at the end of the circuit whose output is then given to the NOR gate to reset when both output go high at the same time. The flip-flops have the same design, one of them will control the UP output of the PFD and the other will control the DOWN output. Fig.4 shows a schematic design of the NOR gate.

Table 1- Dead Zone And Power Consumption For Different Architecture

Architecture	Dead Zone	Power Consumption
Traditional PFD	76PS	1.16mA(2.08mW)
Modified PFD	64PS	334.8uA(0.602mW)
DEC- PFD	10PS	132.6uA(0.238mW)

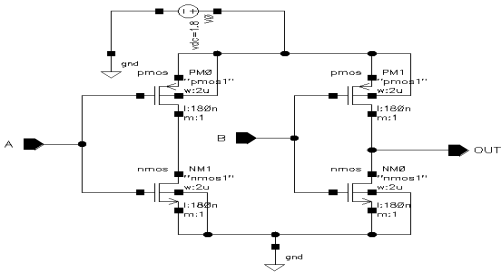

Fig. 4- Schematic Design of the NOR Gate

Due to the NOR reset path, the time needed to charge the NOR gate and reset both flip-flops will be added to the reset delay time in the internal components of the flipflops and produce a large dead zone.

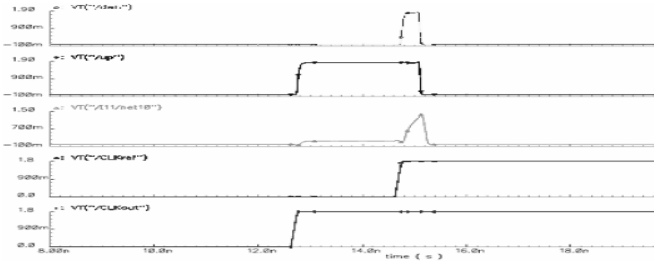

Fig. 5- Dead zone by NOR reset Delay

Fig.5 illustrates the simulated result for large dead zone for this design. NOR gate needs around 76 Pico seconds to be able to reset both flip-flops, and because of this delay both outputs will be high at the same time, therefore they will switch on both transistors in the charge pump preventing it from charging the output up or down according to this phase error of the input signals.Fig.6 shows the simulation result for the traditional PFD.

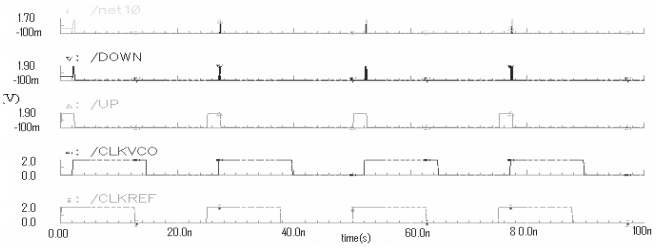

Fig. 6- Simulation of traditional PFD with 4ns delay

The input clock frequency is 100MHz with CLKREF leading CLKVCO by 4ns this result in generation of an UP signal. The power consumption of the PFD is 2.08mW @ 100 MHz which is a high value and that is due to the reset path that consumes some power to charge up and reset both flip-flops.

Modified PFD Architecture

The Traditional PFD Architecture has large deadzone and high power consumption due to the reset path and the components involved [6]. For reducing deadzone and power consumption the reset path was omitted and the CLK signal was applied to the RST input for each flip-flop to reset them as soon as both flip-flops have high output at the same time. Fig.7 shows the block diagram of the modified PFD architecture. The simulation result of the modified PFD shows that the dead zone of this design is 64 ps, and the power consumption of the PFD is 2.08mW @ 100 MHz which makes it a better candidate for phase locked loop system design than

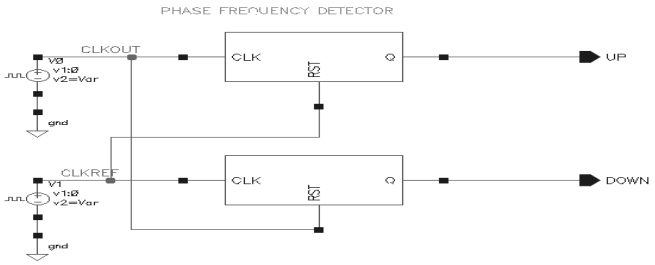

Fig. 7- Block diagram of modified PFD Architecture

the traditional PFD, beside the lower power consumption make this design more suitable for handheld devices like PDA, Cell phones that use a limited power supply. Fig.8 shows dead zone for modified PFD.

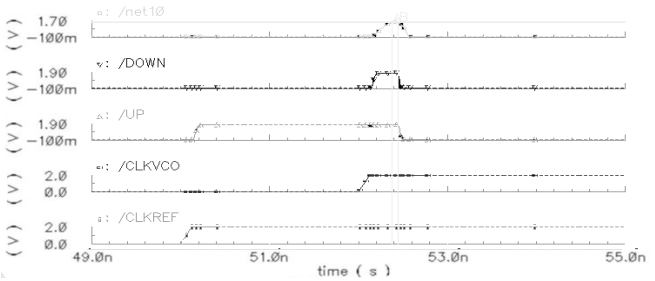

Fig. 8- Dead Zone for modified PFD

Double Edge Checking PFD Architecture

To achieve a higher speed PFD than the modified an another design is proposed which depends on detecting the raising and falling edge of the input signals [7]. Fig.9 shows the schematic design of the double edge checking PFD architecture. Instead of feedback reset path, both CLK signals will reset both outputs as soon as they are high at the same time [8]. This circuit operates as follow, when CLKOUT raises both node 1 and 2 will become low.

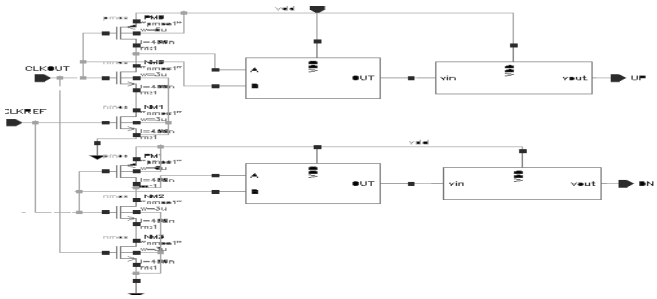

Fig. 9- Schematic design of Double edge checking PFD

As CLKREF goes up node changed from low to high, same as when CLKOUT charges to high node 1 changed from low to high. The output is the given to NAND gate followed by an inverter [8]. Fig.10 shows the simulation result of this PFD.

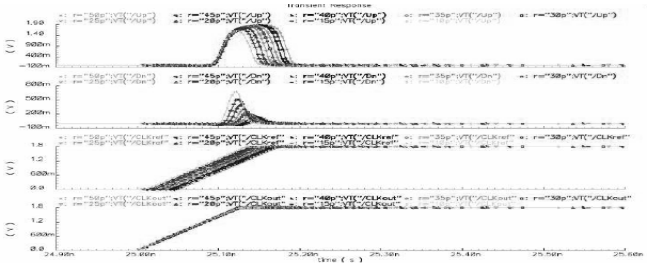

Fig. 10- Dead Zone in DEC-PFD

The dead zone of this design is only 10ps which is almost near to having zero dead zone. The power consumption of the DEC PFD is 0.238mW @ 100 MHz.

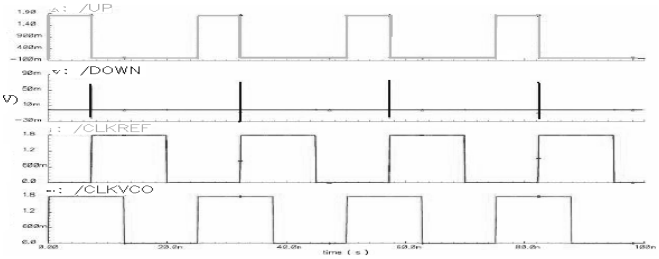

Fig. 11- DEC-PFD with 680ps delay

Fig.11 shows a simulation of this PFD at 100MHz and CLKOUT leading CLKREF by 750ps; this will result in an UP signal, while the DOWN signal will be low all the time. The simulated results for all the three architecture are tabulated.

Conclusion

The three architectures have been simulated for deadzone and power consumption. For application involving low power consumption and less deadzone the double edge checking architecture is the best potential candidate. The simulation result of dead-zone value is 3-ps and maximum operating frequency can up to 2.4 GHz. This circuit can be used in the application on high frequency, low deadzone and low power phase locked loop.

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