Implementation of threshold logic gates using RTDs

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Abstract-In this paper, Threshold logic gates (TLG) are implemented using Resonant Tunneling Diodes (RTD). TLG is conceptually similar to the early McCulloch-Pitts model of the neuron and is normally used to implement linearly separable binary functions. RTD has demonstrably promising electronic features due to its high speed switching capability and functional versatility. Great circuit functionality can be achieved through integrating field-effect transistors (FET) in conjunction with Resonant Tunneling Diodes to modulate effective negative differential resistance (NDR) of the RTD. RTDs are intrinsically suitable for implementing threshold logic rather than Boolean logic, which has dominated CMOS technology in the past. The basic functional unit in the proposed implementation is the monostable-bistable transition logic element (MOBILE). Commonly used logic functions like the OR, AND, and MAJORITY function have been implemented and tested through SPICE simulation.
Keywords- threshold logic, resonant tunneling diode (RTD), MOnostable BIstable Latch Enable (MOBILE)

I. INTRODUCTION

The schematics of a biological neuron and a TLG/artificial neuron are shown in figures 1(a) and 1(b) respectively. The basic operating principles of a TLG are similar to the early McCulloch-Pitts model of an artificial neuron [1]. TLGs are simulated using circuit models of RTD and FET in SPICE. The models are derived from piecewise linear isation of the I-V characterstics of these devices [2,3,4,5]. The principle of operation of the proposed logic gates is based on monostable bistable latch enable(MOBILE), which is a well documented technique employing the latching capability of RTD [6,7]. Two input AND gate and majority gate are designed and tested. The circuit demonstrates how small-scale threshold logic gates implementing standard Logic functions can be used to replace conventional Boolean gates and achieve reduced circuit complexity.

II. THRESHOLD LOGIC

The elementary nerve cell is called a neuron. Each neuron has a soma or cell body, which contains the cell's nucleus. Each neuron is connected through its main communication links to thousands of other neurons. These links are
(i) Set of dendrites- which are a tree like structure that spread out from the cell. The neuron receives its input electrical signals along these dendrites.
(ii) A single axon-which carries an electrical signal away from the soma to other neurons for processing.
The earliest model of the neuron was given in 1943 and is known as the McCulloch-Pitts model [1]. This model formed the basis for implementing artificial neurons in Artificial Neural Networks (ANN). Table 1 shows the analogy between a biological and an artificial.

Table 1- Analogy between Biological neuron and artificial neuron

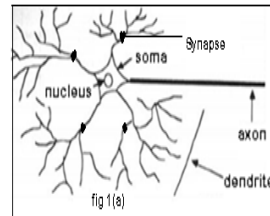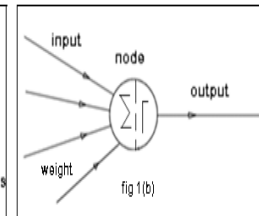| Biological neuron	Artificial neuron
Soma Dendrites Axon Synapse	Node Inputs Output Weight

fig1(a) biological neuron

fig 1(b) artificial neuron

Threshold logic is equivalent to the McCulloch-Pitts model of a neuron. It computes the weighted sum of its inputs and compares the sum with a threshold value.

$f(x) = 1$ if $W_i X_i \geq T$
$\quad = 0$ otherwise

where
W_i=weights; $\quad$ i =1,2…n
X_i= inputs
T =Threshold

Table - 2
Example to illustrate Threshold Logic

X1	X2	X3	F	Weighted sum - T
0	0	0	1	1.5
0	0	1	0	-0.5
0	1	0	1	2.5

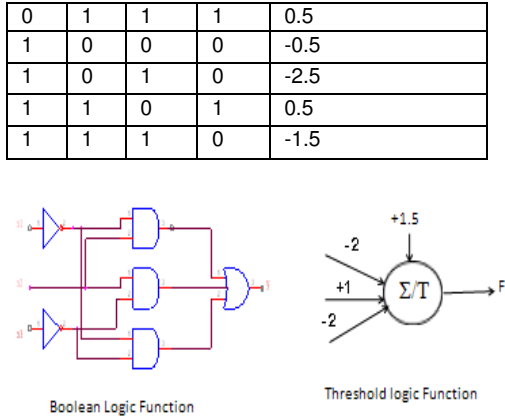|				
0	1	1	1	0.5
1	0	0	0	-0.5
1	0	1	0	-2.5
1	1	0	1	0.5
1	1	1	0	-1.5

Fig. 2- Comparison between Boolean logic and threshold logic implementation

III. RESONANT TUNNELING DIODE

The RTD schematic symbol and its I-V curve are shown in Figure 3(a) and 3(b) respectively. RTD devices feature a nonlinear I-V characteristic that exhibits a region of negative differential resistance (NDR). When current I_{RTD} is smaller than its peak value I_P, it increases as V_{RTD} increases. The RTD is at a low resistance state. Once I_{RTD} reaches I_P, the RTD enters the NDR region and I_{RTD} decreases as V_{RTD} increases. The RTD switches to a high resistance state. Many important circuit functionalities can be enabled by exploiting this special NDR characteristic. [10]
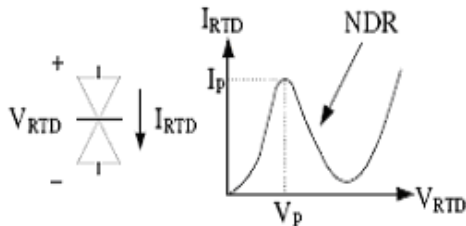

Fig. 3(a)- RTD schematic symbol (b) I-V characteristics

The elementary unit of RTD based threshold logic gate (TLG) is the MOnostable BIstable Logic Element (MOBILE). It consists of two RTDs driven by a V_{bias} as shown in fig. 4. Circuit applications of RTDs are mainly based on the MOBILE [11].

When V_{bias} is low both RTDs are in ON state. With increasing V_{bias}, device with lowest peak current switches from ON state to OFF state.

Output is HIGH if driver switches.
Output is LOW if load switches.

Peak currents are proportional to RTD Areas λ_1 & λ_2.
If $\lambda_1 < \lambda_2$ $V_{out} = 0$
If $\lambda_2 < \lambda_1$ $V_{out} = 1$

Logic functionality can be achieved if the peak current of one of the RTDs is controlled by an input.
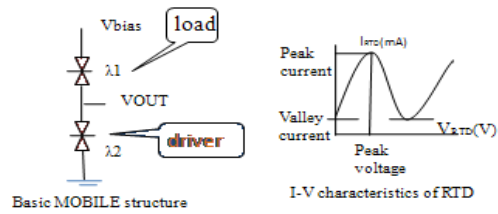

Fig. 4(a)- Basic MOBILE structure (b) I-V characteristics of RTD

IV. GENERIC MOBILE THRESHOLD GATE
RTD areas determine the weights W_i. For positive weight, RTD-HFET is placed in upper circuit (load) and for negative weight it is placed in lower circuit (driver).
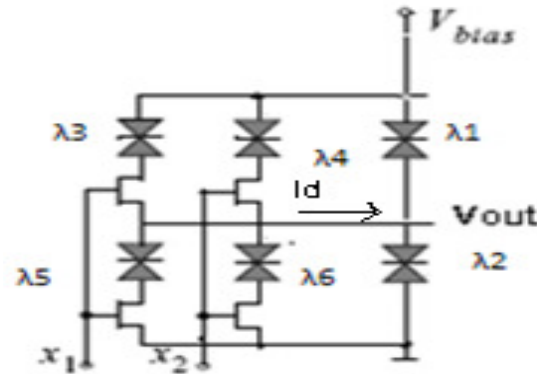

Fig. 5- General MOBILE circuit
The output is 1 when
$I_d - I_t \geq 0$
i.e.
$(W_1X_1 + W_2X_2 - W_3X_3 - W_4X_4)$ A I_{pd} - T A $I_{pd} \geq 0$
When
$W_1X_1 + W_2X_2 - W_3X_3 - W_4X_4 \geq T$,
$V_{out} = 1$
Otherwise $V_{out} = 0$
Where $W_1 = \lambda_3$, $W_2 = \lambda_4$, $W_3 = \lambda_5$, $W_4 = \lambda_6$ and A is the area of RTD.

V. DESIGN OF THRESHOLD LOGIC GATES
AND Function

Table 3- Binary representation of AND function

X_1	X_2	F
0	0	0
0	1	0
1	0	0
1	1	1

INPUTS: {X_1, X_2}
CONDITIONS:
Both inputs are zero:

$I_d - I_t < 0$
$(W_1X_1+W_2X_2)\ A\ I_{pd} - TA\ I_{pd} < 0$
$(W_1X_1+W_2X_2) - T < 0$
$(W_1X_1+W_2X_2) < T$
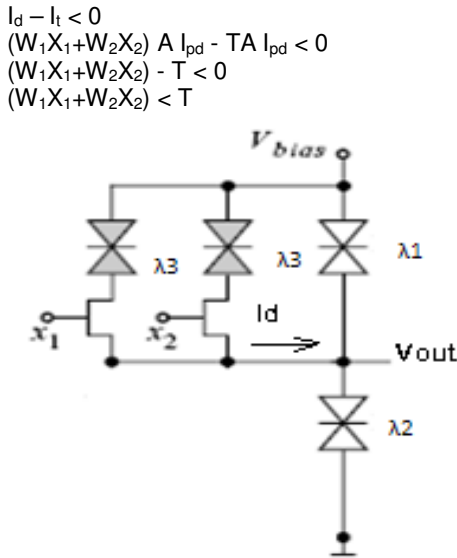

Fig 6-AND function implementation

Putting $T = \lambda_2-\lambda_1$, $W_1=\lambda_3$, $W_2=\lambda_3$,
$X_1 = X_2=0$
$\lambda_1< \lambda_2$

(ii) One input is one:
$I_d - I_t < 0$
$(W_1X_1+W_2X_2)\ A\ I_{pd} - T\ A\ I_{pd} < 0$
$(W_1X_1+W_2X_2) -T < 0$
$(W_1X_1+W_2X_2) < T$

Putting $T = \lambda_2-\lambda_1$, $W_1=\lambda_3$, $W_2=\lambda_3$
$X_1 =0$, $X_2= 1$ *or* $X_1 =1$, $X_2 =0$
$\lambda_3 < \lambda_2-\lambda_1$
$\lambda_2 > \lambda_1+ \lambda_3$

(iii) Both inputs are one
$I_d - I_t > 0$
$(W_1X_1+W_2X_2)\ A\ I_{pd} - T\ A\ I_{pd} > 0$
$(W_1X_1+W_2X_2) -T > 0$
$(W_1X_1+W_2X_2) > T$

Putting $T = \lambda_2-\lambda_1$, $W_1=\lambda_3$, $w_2=\lambda_3$, $X_1 = X_2=1$

$2\lambda_3 > \lambda_2-\lambda_1$
$\lambda_2 < \lambda_1+2 \lambda_3$

Hence, the conditions for AND function realization are

$\lambda_1< \lambda_2$
$\lambda_2 > \lambda_1+ \lambda_3$
$\lambda_2 < \lambda_1+2 \lambda_3$

The above conditions can be satisfied by taking
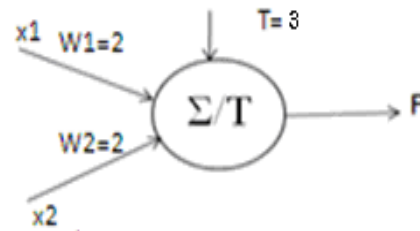
$W_1=W_2=2$, $T=3$ ($\lambda_2=4$, $\lambda_1=1$)

Fig. 7- Implementation of threshold logic AND gate

(2) Majority Function
Table 4-Binary representation of majority function

X_1	X_2	X_3	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

INPUTS: $\{X_1, X_2\}$

CONDITIONS:
(i)Three inputs are zero
$I_d- I_t < 0$
$(W_1X_1+W_2X_2+W_3X_3)\ A\ I_{pd} < T\ A\ I_{pd}$
$W_1X_1+W_2X_2+W_3X_3 <T$
Putting $T = \lambda_2-\lambda_1$, $W_1=W_2=W_3=\lambda_3$
$X_1=X_2=X_3=0$
$\lambda_1< \lambda_2$

(ii) One input is one
$I_d - I_t <0$
$(W_1X_1+W_2X_2+W_3X_3)\ A\ I_{pd} - T\ A\ I_{pd} < 0$
$(W_1X_1+W_2X_2+W_3X_3) -T <0$
$(W_1X_1+W_2X_2)+W_3X_3 <T$

Putting $T = \lambda_2-\lambda_1$, $W_1=\lambda_3$, $w_2=\lambda_3$
$X_1 =1$, $X_2= 0$, $X_3=0$ *or* $X_1 =0$, $X_2= 1$, $X_3=0$ *or* $X_1 =0$, $X_2= 0$, $X_3=1$
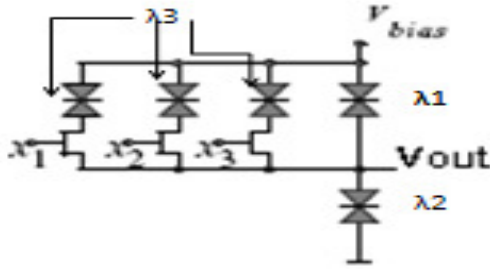$\lambda_2 -\lambda_1 > \lambda_3$
$\lambda_2 > \lambda_1+ \lambda_3$

Fig 8- Circuit of Majority Function

(iii) Two inputs are one
$I_d - I_t > 0$
$(W_1X_1 + W_2X_2 + W_3X_3) \, A \, I_{pd} - T \, A \, I_{pd} > 0$
$(W_1X_1 + W_2X_2 + W_3X_3) - T > 0$
$(W_1X_1 + W_2X_2) + W_3X_3 > T$

Putting $T = \lambda_2 - \lambda_1$, $W_1 = \lambda_3$, $W_2 = \lambda_3$
$X_1 = 1$, $X_2 = 0$, $X_3 = 0$ or $X_1 = 0$, $X_2 = 1$, $X_3 = 0$;
or $X_1 = 0$, $X_2 = 0$, $X_3 = 0$
$\lambda_2 - \lambda_1 < 2\lambda_3$
$\lambda_2 < \lambda_1 + 2\lambda_3$

(iv) Three inputs are one
$I_d - I_t > 0$
$(W_1X_1 + W_2X_2 + W_3X_3) \, A \, I_{pd} - T \, A \, I_{pd} > 0$
$(W_1X_1 + W_2X_2 + W_3X_3) - T > 0$
$(W_1X_1 + W_2X_2) + W_3X_3 > T$

Putting $T = \lambda_2 - \lambda_1$, $W_1 = \lambda_3$, $W_2 = \lambda_3$
$X_1 = 1$, $X_2 = 0$, $X_3 = 0$ or $X_1 = 0$, $X_2 = 1$, $X_3 = 0$;
or $X_1 = 0$, $X_2 = 0$, $X_3 = 0$
$\lambda_2 - \lambda_1 < 3\lambda_3$
$\lambda_2 < \lambda_1 + 3\lambda_3$
Hence, the conditions for Majority Function realization are

$\lambda_1 < \lambda_2$
$\lambda_2 > \lambda_1 + \lambda_3$
$\lambda_2 < \lambda_1 + 2\lambda_3$
$\lambda_2 < \lambda_1 + 3\lambda_3$

The above conditions can be satisfied by taking

$W_1 = W_2 = W_3 = 2$, $T = 3$ ($\lambda_2 = 4$, $\lambda_1 = 1$)

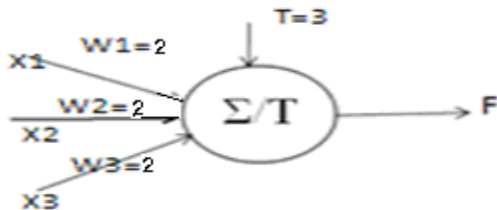Fig. 9- Implementation of threshold logic majority function
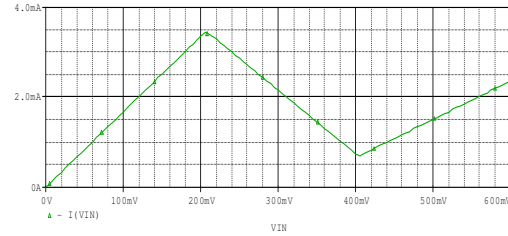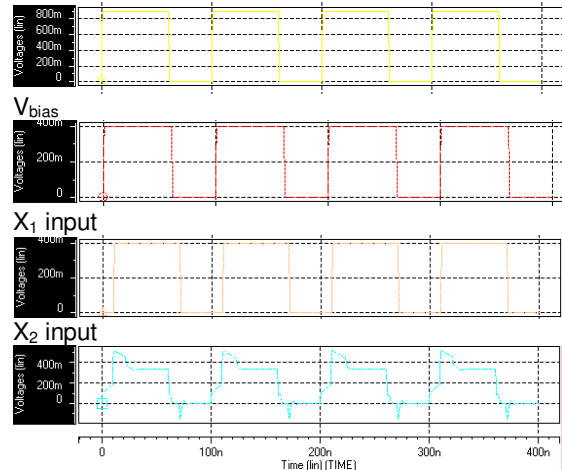
VI. SIMULATION RESULTS

Fig. 10- RTD characteristics

V_{bias}

X_1 input

X_2 input

V_{out}

Fig. 11-AND function implementation results

VII. CONCLUSION

In this work, TLGs based circuits have been successfully implemented using RTDs. It has been found that TLGs based circuits exhibit correct functionality and a robust circuit operation under device parameter and bias voltage variation. The inherent low complexity of RTD based threshold logic gates allows for gains in function density. Due to operation of RTD/HFET in Giga Hertz regime, RTD/HFET based nanoscale circuits have great potential to be used in high performance digital signal processing.

REFERENCES

[1] McCulloch W.S. and Pitts W. (1943) *Bulletin of Mathematical Biophysics*, 5, 115-133.
[2] Santoro R.P. (1995) *IEEE Trans. Edu.*, 38, 107–117.
[3] Mayukh Bhattacharya and Pinaki Mazumde (2001) *IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems*, 20, 39-50.
[4] Kuo T.H., Lin H. C., Anandakrishnan U., Potter R. C. and Shupe D. (1989) *IEEE Int. Electron Devices Meeting Tech. Dig.*, 567–570.

[5] Mohan S., Sun J. P., Mazumder P. and Haddad G. I. (1995) *IEEE Trans. Computer-Aided Design,* 14, 653–662.

[6] Rui Zhang, Pallav Gupta, Lin Zhong, and Niraj K. Jha (2005) *IEEE transactions on computer-aided design of integrated circuits and systems*, 24, 1.

[7] Marek A. Bawiec and Maciej Nikodem (2009) *Logic Function Synthesis for Generalized Threshold Gate Circuits, The Institute of Computer Engineering, Control and Robotics, Wroclaw University of Technology, San Francisco, California, USA, Poland DAC'09,* 253-260.

[8] Pettenghi H., Avedillo M. and Quintana J. (2008) *IEEE International Symposium on Circuits and Systems*, 2350–2353.

[9] Tom P. E. Broekaert, Berinder Brar, J. Paul A. van der Wagt, Alan C. Seabaugh, Frank J. Morris, Theodore S. Moise, Edward A. Beam, September 1998 Ireland Gary, A. Frazier. *IEEE journal of solid-state circuits*, 33, 9.

[10] Kelly P.M., Thompson C.J., Mc Gnnity T.M., and Maguire L.P. (2003) *IWANN,* 41–48.