Journal of Electronic and Electrical Engineering
ISSN: 0976–8106 & E-ISSN: 0976–8114, Vol. 1, Issue 2, 2010, pp-09-12

Simulation of SOI MOSFET using ATLAS

Mohammad Kaifi, Siddiqui M.J., Abbasi T.A. and Khan M.U.[1]
Department of Electronics Engineering, Aligarh Muslim University, Aligarh, 202002, India
[1]Department of Electrical Engineering, Rameshwaram Institute of Tech. & Management, Lucknow,India

Abstract- Silicon on insulator (SOI) CMOS offers performance gain over bulk CMOS mainly due to reduced parasitic capacitances and latchup. It is most promising technology when low cost low power and low voltage suppply is required. kink effect and self heating are two important points of concern in case of SOI MOSFET. In this paper we first briefly discuss the SOI technology, kink effect and lattice heating in SOI MOSFET's and then we present the simulation results obtained using the industry standard software ATLAS from SILVACO.
Keywords-Silicon on insulator, SOI MOSFET, Kink effect, ATLAS, Lattice heating

Introduction

Silicon is the most commonly used material in contemporary IC technology. In a modern day IC there may be millions of transistors on a small piece of silicon. Naturally the fabrication and design of these IC's cannot be done without computer aids. Both the fabrication and design of these IC's require Electronic Design Automation tools(EDA). There is a need for highly precise software tools to analyze and simulate the design and fabrication of integrated circuits. Lot of research has been done and still going on these issues. As a result we have got highly useful tools for design and fabrication of IC's. CMOS technology has been the driving technology for whole microelectronics industry for last many years. But the major problem associated with cmos is the parasitic capacitances which becomes prohibitively large as we goto lesser channel lengths. So people have proposed various ideas to counter this problem. One of the solution is Silicon On Insulator(SOI) technology. In silicon on insulator technology small islands of silicon are formed on an insulator film. Circuits are fabricated on these islands of silicon. Using SOI fabrication process coupled with lateral isolation techniques we can get circuits with very small parasitic capacitances and latchup free circuits.

Silicon on insulator technology

CMOS integrated circuits are almost exclusively fabricated on bulk silicon substrates for two well known reasons: the availability of electronic-grade material and because a good quality oxide can be readily grown on silicon, a process which is not possible on germanium or on compound semiconductors. Yet modern MOSFET's made in silicon are far from the ideal structure. Bulk MOSFET's are made in silicon wafers having a thickness of approximately 800micrometers but only the first micrometer at the top of the wafer are used for transistor fabrication. Interactions between the devices and the substrate give rise to a range of unwanted parasitic effects.
One of these parasitic is the capacitance between diffused source and drain and substrate. This capacitance increases with substrate doping and becomes larger in modern submicron devices where the doping concentration in the substrate is higher than in previous MOS technologies. In addition latchup which consist of the unwanted thyristor inherently present in all bulk CMOS

structures becomes a serious problem in devices with small dimensions. The solution is SOI MOSFET.
The SOI MOSFET contains the traditional three terminals (source, drain and gate which controls a channel in which current flows from source to drain). However the full dielectric isolation of devices prevents the occurrence of most of the parasitic effects experienced in bulk silicon devices. Most parasitic effects in bulk MOS devices find their origin in the interactions between the device and the substrate. Latch up in bulk devices finds its origin in the PNPN structure of the CMOS inverter. The latchup can be symbolized by two bipolar transistors formed by the substate, the well and the source and drain junctions. For latchup to occur the current gain of the loop formed by the two transistors should be greater than one. In an SOI CMOS inverter the silicon film containing the active devices is thin enough for the junction to reach through to the buried insulator. A latchup path is ruled out because there is no current path to the substrate. In addition the lateral PNPN structures contain heavily doped bases that virtually reduce the gain of the bipolar devices to zero.

SOI MOSFET

The MOSFET is the most widely used SOI device. SOI MOSFET's exhibit interesting properties that make them particularly attractive for applications such as radiation hard circuits and high temperature electronics.
The physics of the SOI MOSFET is highly depended on the thickness and doping concentration of the silicon film in which they are made. Two types of devices can be distinguished : devices in which the silicon film in the channel region is never completely depleted called partially depleted MOSFET or PD MOSFET. The other type of device where silicon film can be completely depleted is called fully depleted MOSFET or FD MOSFET.
In PD MOSFET the silicon film thickness is larger than twice the value of maximum depletion width. In such a case there is no interaction between the depletion zones arising out from the front and back interfaces. A neutral region exists beneath the depletion regions. If this neutral peace of

Copyright © 2010, Bioinfo Publications,

silicon called body is connected to ground by a body contact the characteristic of the device will be exactly those of a bulk device.
In a FD MOSFET the silicon film thickness is smaller than maximum depletion width. In this case the silicon film is completely depleted at threshold, irrespective of the bias applied at the back gate.

Kink Effect

The kink effect is characterized by the appearance kink in the output characteristics of an SOI MOSFET. The kink appears above a certain drain voltage. It is not observed in bulk devices at room temperature when substrate or well connections are provided but it can be observed in bulk MOSFET's operating at low temperatures
Kink effect can be explained as follows. Consider a partially depleted SOI n-channel transistor. When the drain voltage is high enough, the channel electrons can acquire sufficient energy in the high electric field zone near the drain to create electron-hole pairs, due to impact ionization mechanism. The generated electrons move rapidly into the channel and the drain while the hole migrates towards the place of lowest potential i.e. floating body. The injection of holes into the floating body forward biases the source-body diode. The increase of the body potential gives rise to a decrease of threshold voltage. This decrease of threshold voltage induces an increase of the drain current as a function of drain voltage which can be observed in the output characteristics of device as a kink.

Lattice Heating

SOI MOSFET's are thermally insulated from the substrate by the buried insulator. As a result , removal of excess heat generated within the device is less efficient than in bulk, which results in substantial elevation of device temperature. The conduction paths for excess heat are multiple: heat diffuses mostly vertically through the buried oxide but some of it through the silicon island into the contacts and metallization.
Due to self heating , a negative resistance can be seen in the output characteristics of SOI MOSFET. It is due to mobility reduction effect caused by the elevation of temperature. This effect is clearly visible on the output characteristics if sufficient power is dissipated in device. Because of the relatively low conductivity of oxide layer, device can heat up by 50-100 degrees and mobility reduction is observed. This effect has been included in device and circuit simulators.

Subthreshold slope

The inverse subthreshold slope is defined as the inverse of the slope of the Id(Vg) curve in the subthreshold regime, presented on a semilogarithmic plot.
On a log plot the subthreshold current appears as a straight line. The inverse of the slope of that line is called inverse subthreshold slope or simply subthreshold slope. It is expressed in volts per decade. The lower the value of subthreshold slope, S, the more efficient and rapid the switching of the device from the off state to on state

SILVACO TCAD

Technology–Computer Aided Design (TCAD) is one of the most commonly used simulation tools. It helps the engineers to save time, cost and also reduce the Complexity of the original design during the designing process using the available detail of the semiconductor properties. This is a very powerful tool as it could show the result as close as the actual process.
This simulation tool does not require any applied of complicated formula to be put into for simulation and the command were more easy to understand. The software was able to simulate the carriers in the devices or materials. This simulation software is able to model the two dimensional on the electrical characteristics when bias condition is applied. It shows the amazing side of the modern technologies.
ATHENA is the process simulator, which is used to predict the physical structures of the processing steps. As for ATLAS, is a tool that used to predicts the electrical characteristics associated with the specified bias conditions. However, ATLAS also has the same feature as ATHENA to construct the structure of the device but only in a simple form. The UTMOST device characterisation and modelling software can use the electrical characteristic predicted by ATLAS. The compact model make used of the simulated device characteristics for the engineers to do a preliminary circuit designs.
ATLAS is a physical-based device simulator used for device simulation, which have 3 major advantages. They are predictive; provide insight and captures theoretical knowledge that will benefit the non-experts. This device simulation problem by defining

A. The physical structure to be simulated
B. The physical models to be used
C. The bias conditions for which electrical characteristics are to be simulated.

Simulation results

SUBTHRESHOLD SLOPE: We simulated the SOI MOSFET for both partially depleted and fully depleted case. The buried oxide thickness was taken as 0.4um and gate oxide thickness as 17nm. Gate length was 500nm. The silicon layer on buried oxide is 0.2um for partially depleted case and 0.1um for fully depleted case. The subthreshold slope is found to be 107mV/dec for partially depleted and 72mV/dec for fully depleted case.

KINK EFFECT: We simulated the SOI MOSFET on a silicon layer of 0.3um over 0.4um thick buried oxide layer. We observe a prominent kink in the Id-Vds curve as the drain voltage is increased.

LATTICE HEATING: We have done simulation to plot the Id-Vds curve for two cases. In one case we consider the lattice heating by using model of lattice heating in simulation. In second case we neglect self heating. Gate length is 500nm.It is observed that in case of self heating drain current decreases as drain voltage is increased so we are getting negative transconductance

Conclusion

In this work we have studied the basic principles related with SOI MOSFET. We simulated the characteristics of SOI MOSFET and found the effect of lattice heating and kink effect. By the help of simulations we gained better comprehension of theoretical fundamentals of SOI MOSFET.

By getting the understanding the working of SOI MOSFET and SILVACO we can do some good research. We have done 2-D simulation , 3-D simulation may also be done on similar lines. Leakage current may also be simulated. Breakdown phenomenon in SOI MOSFET can be simulated. Various mathematical models are proposed in literature for kink effect in SOI MOSFET we can verify them. These models can be further improved.

References

[1] Coligne J.P. *Silicon on Insulator Technology: Materials for VLSI, 2nd ed. Kluwer Academic Publishers.*

[2] Silvaco Manual Dasgupta. *Semiconductor Devices:Modelling and Technology, PHI.*

[3] Rabaey, *Digital Integrated Circuits,2nd ed. Pearson education, PHI.*

[4] Campbell, *The Science and Engineering of Microelectronic Fabrication, 2nd ed , Oxford University Press.*

[5] Tsividis, *Operation and Modelling of MOS Transistor, TMH*

[6] Shahidi (2002) *IBM J. RES & DEV* VOL.46.

[7] Siddiqui M.J., *"A proposed model for Kink effect in SOI MOSFET", Proc of MTECS-2008.*

Copyright © 2010, Bioinfo Publications,

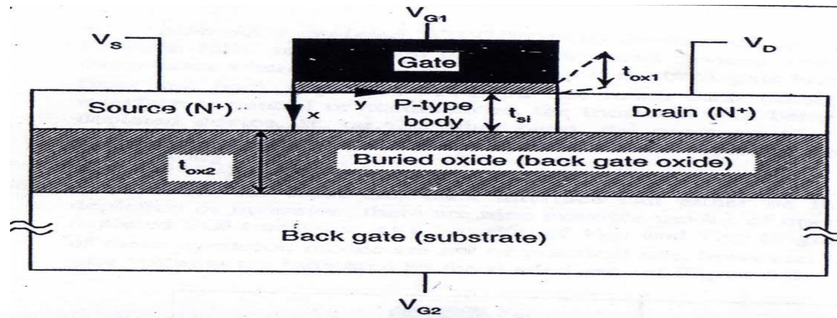

Fig. 1- schematic cross section of n-channel SOI MOSFET

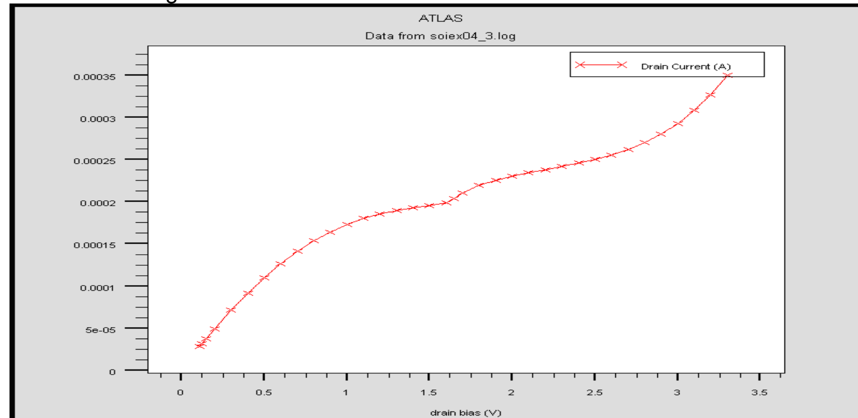

Fig.2- Id-Vds curve showing kink effect

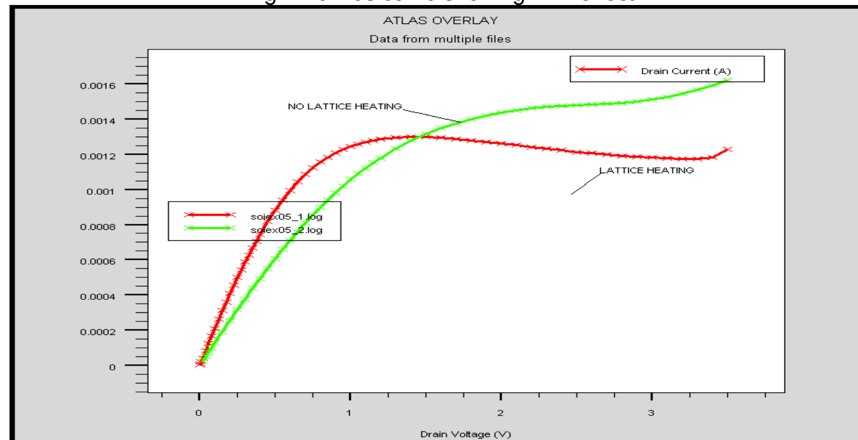

Fig.3- Effect of lattice heating

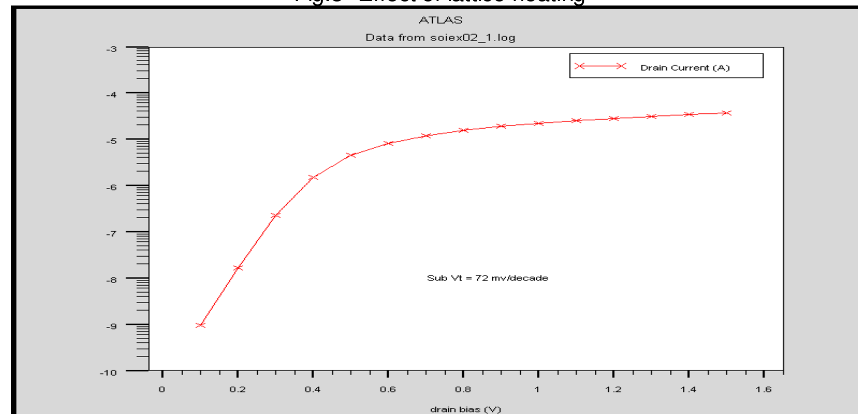

Fig. 4-(below) subthreshold curve for fully depleted MOSFET