Design and optimization of Patch Antenna for WLL-Cor-DECT Technology using IE3D



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Abstract-In this paper, we present a patch antenna for WLL- Cor-DECT Technology with resonance frequency of 1.88 GHz. The dielectric material selected for my design is Silicon which has a dielectric constant of 11.9. A substrate with a high dielectric constant has been selected since it reduces the dimensions of the antenna. For the microstrip patch antenna to be used in WLL System, it is essential that the antenna is not bulky. Hence, the height of the dielectric substrate is selected as 31 mil patch along with a single feed. The input impedance and return loss of the patch antenna are 388Ω and 5.8 dB, respectively. From the optimized results obtained, we get the return loss of below 35 dB at resonant frequency. **Keywords-** WLL-Cor-DECT, microstripline Patch antenna, Single feed, Input impedance, return loss, smith

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INTRODUCTION

The Wireless in local loop digitally enhanced cordless technology (WLL-Cor-DECT) uses the frequency range from 1880-1900 MHz. we prefer DECT because the Cost of setting up traditional copper based telephone networks very high Wireless reduces the cost of Access part of network which consists of 70% of total costs. DECT is a simple technology structure, easier to implement, supports large number of subscribers Costs less than traditional Wireless Structure used by Mobile Operators. Hence the antenna designed must be able to operate in this frequency range. The resonant frequency selected for my design is 1.88 The transmission line model is used to GHz. design the rectangular patch antenna.

In certain applications, such as high data-rate wireless transmission, this low bandwidth is not adequate. In order to meet the demand for larger bandwidth, several techniques have been reported; the most commonly employed technique is increasing the thickness of the substrate supporting the microstrip patch. However limitations still exist on the ability to effectively feed the patch on a thick substrate and the radiation efficiency can degrade with increasing substrate thickness Traditional single layer singly fed microstrip patch antennas have inherent limitations in gain, impedance and axial-ratio bandwidths. This is mainly owing to the resonant nature of the patch antennas. One way to increase the impedance bandwidth is by minimizing the unloaded Q-factor with the use of an electrically thick substrate for the patch[2]. In this paper, we do the optimization of the structure to achieve the return loss from 5.8dB to below 35dB at 1.88GHz frequency. Highly efficient and electrically small

antennas for microwave and millimeter-wave are needed due to the increasing demand for cellular, satellite, and advanced wireless communications.

DESIGN AND ANALYSIS OF PATCH

For microstrip antennas, the width (W) and length (L) of the radiating patch and the effective permittivity of the microstrip



Fig. 1-The illustration of a simple edge-fed patch antenna

Structure (\mathcal{E}_{re}) which support the operation at the required resonant frequency (or the free-space wavelength λ_0) can be designed as follows, using the formulas given in [1].

$$W = \frac{c}{2f_o\sqrt{\frac{\mathcal{E}_{re}+1}{2}}} \qquad \dots (1)$$

$$L = \frac{c}{2f_o \sqrt{\varepsilon_{re}}} - 2\Delta L \qquad \dots (2)$$

Where,

$$\Delta L = 0.412h \frac{\left(\varepsilon_{re} + 0.3\right)\left(\frac{W}{h} + 0.264\right)}{\left(\varepsilon_{re} - 0.258\right)\left(\frac{W}{h} + 0.8\right)} \quad \dots (3)$$

and

$$\mathcal{E}_{re} = \frac{\mathcal{E}_r + 1}{2} + \frac{\mathcal{E}_r - 1}{2} \left[1 + 12 \frac{h}{W} \right]^{-1/2} \dots (4)$$

Using equation (3) we can calculate the length ΔL and by equation (4) we calculate the effective dielectric constant, which helps to find out the L using equation (2)

Table 1.1 The parameters of the patch antenna

Substrate	31 mils	Dielectric	11.9
Thickness		Constant	
Patch	1512	Patch	1500
Length, L	mils	Width, W	mils
Inset Width,	115	Inset	452
S	mils	Depth, D	mils
Strip Width,	60 mils	Feed Line	750
Т		Length, F	mils



Fig. 2(a)- Simulated Return loss plot for the rectangular patch antenna



Fig. 2(b)- Simulated Z-Parameters plot for the rectangular patch antenna



Fig. 2(c)- Simulated smith chart for the rectangular patch antenna

As you can see, in Fig 2(a) the resonance is not exactly at 1.88 GHz. It is resonating at about 1.87 GHz with best return loss as 5.8 dB. Fig 2(b) & Fig 2(c) represents the input impedance and smith chart respectively as we see, the resonance is not exactly at 1.88 GHz. It is resonating at about 1.87 GHz with best return loss as 5.8 dB.for which we have to go for optimization

OPTIMIZATION

For the antenna we are discussing, we can adjust the length L to change the resonant frequency. We can adjust the inset depth D to tune the matching. Also, both variables are not independent or changing L may change the matching and changing D may change the resonance. If they are

2

independent, we can optimize one dimension at a time and it may make an optimization much easier. Our goals are: Re[S(1,1)] = 0 and Im[S(1,1)] = 0 at 1.88 GHz. we want to optimize this antenna to a perfect match at 1.88 GHz.By defining the variable bounds for the vertices as Low bound -100 & -200 and high bound 100 & 200.We optimized the geometric structure for 1.88 GHz resonant frequency.here we have selected the POWELL scheme for optimization



Fig. 3- The trends and bounds of the variable.



Fig. 4(a)-Comparison in S-parameters between original and optimized structures.

Z-Parameters Display



Fig. 4(b)- Optimized Z parameter plot for the rectangular patch antenna



RESULTS AND DISCUSSIONS

Fig. 2(a) shows the measured return loss for the rectangular patch antenna shown in fig 1. The rectangular radiating patch was of dimensions 1512 mil x 1500 mil (L x W). From the optimized result obtained in fig. 4(a), it is seen that the patch antenna is radiating at a frequency of 1.88GHZ with the desired return loss for personal communication system.

CONCLUSION

The present work presents a rectangular microstrip patch antenna. A slot of calculated dimension is etched out of the conventional antenna to reduce spurious response though there is a minor shift in the operating frequency. The overall improved response justified the new design attempt. which can be used in WLL-Cor-DECT system

ACKNOWLEDGMENT

The authors would like to thank authorities of Ideal Institute of Technology for all the support provided.

REFERENCES

- Balanis C. A. (2005) Antenna theory, analysis and design, 3rd edition, John Wiley & Sons, Inc.PP 843 – 865.
- [2] Ramesh Garg, Prakash Bhartia, Inder Bahl, Apisak Ittipiboon (2001) Microstrip antenna Design Handbook, Artech House, Boston, London, 2001.
- [3] Pozar D. M. (1992) Microstrip antennas, IEEE proc. Antenna Propag., 80, 79-81.
- [4] Wong K.L. (1999) Design of Nonplanar Microstrip Antennas and Transmission Lines, John Wiley & Sons, New York.
- [5] Amman M. (1997) Design of Rectangular Microstrip Patch Antennas for the 2.4 GHz Band, Applied Microwave & Wireless, 24-34.



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