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IMPLEMENTATION OF QPSK BASED COMMUNICATION SYSTEM ON TMS320C6713 DSK

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Abstract- In this paper, we present two variants of QPSK transmitter/receiver that incorporates the functionalities of digital modulator/ demodulator along with controlling features such as data generation, symbol generation, modulation, demodulation and frame synchronization for both BM and IQ methods. The BER is calculated by passing the modulated wave through the AWGN channel. The standard deviation of the difference between the theoretical and practical BER values is found to be 0.0028 and 0.0031 for BM and IQ method respectively. The simulation and analysis of the proposed model is done on MATLAB and the TMS320C6713 DSK is used for real time implementation.

Keywords- QPSK, BM, IQ, frame synchronisation, AWGN.

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Introduction

When transmission of data is through a band-limited channel, it is always desirable to efficiently use the channel bandwidth, by having a maximum allowable data rate and at the same time having an average probability of error, P_e below a specified value. The Modulation scheme in which bandwidth is conserved is called bandwidth efficient modulation scheme. In digital communication, Quadri-phase-shift keying (QPSK) is one such modulation scheme. In this scheme, for a given binary data rate; there is reduction in transmission bandwidth by a factor of 2. Quadrature means that the signal shifts between phase states which are separated by 90 degrees. The signal shifts in increments of 90 degrees from 45 to 135, -45, or -135 degrees. These points are chosen as they can be easily implemented using I/Q modulator. Only two I values and two Q values are needed and this gives two bits per symbol. Hence there are four states in QPSK. QPSK transmits twice the data rate in a given bandwidth compared to BPSK at the same BER. It is therefore a more bandwidth-efficient type of modulation than BPSK, potentially twice as efficient.

QPSK modulation scheme is power efficient without any compromise in the bandwidth efficiency. QPSK requires less transmitter power than QAM to achieve the same BER [3].

The organization of the rest of this paper is as follows. In section II we discuss the implementation of Balanced Modulation QPSK system, section III describes the implementation of IQ channel based QPSK system, section IV presents proposed frame synchronization algorithm, section V explains the real-time implementation of the proposed model on the TMS320C6713 DSK, the obtained results are explained in section VI and conclusions are drawn in the section VII.

Implementation of Balanced Modulation Quadrature Phase Shift Keying

As with the binary Phase Shift Keying (PSK) this modulation scheme is characterized by the fact that the information carried by the transmitted wave is contained in the phase. In particular, in a Quadrature Phase Shift Keying (QPSK) wave, the phase of the carrier takes on one of four possible values, such as 45^o , -45^o, 135^o and -135^o as shown below in the [Table-1] . The QPSK signal can be represented in time-domain by S_i (t) shown in (1). E is the transmitted signal energy per symbol, T_s is the symbol duration, and f_c is the carrier frequency. Each possible values of the phase correspond to a unique pair of bits called the dibit. Thus for example we may choose the above set of phase values to represent the following set of dibits: 10, 00, 01, and 11.

Table 1- Phases and their corresponding dibits

i	$S_i(t)$	Θ_i	Dibit
1	$S_1(t)$	π/4	1
2	$S_2(t)$	3π/4	0
3	$S_3(t)$	5π/4	11
4	$S_4(t)$	7π/4	10

$$S_i(t) = \begin{cases} \sqrt{\frac{2E}{Ts}}\left[\cos(2\pi fct) + (2i-1)\frac{\pi}{4}\right], & 0 \le t \le T_s \\ 0, & \text{elsewhere} \end{cases} \quad (1)$$

The main aim of the QPSK receiver is to recover/extract the phase angles which were used to modulate the corresponding data dibits and there by the decision can be made to recover the data using the extracted phase angles.

The QPSK signal arriving at the receiver is first multiplied with the pair of orthonormal basis function ϕ_1 (t) and ϕ_2 (t),

$$\phi_1(t) = \sqrt{\frac{2}{Ts}}\cos(2\pi fc\ t) \quad (2)$$

$$\phi_2(t) = \sqrt{\frac{2}{Ts}}\sin(2\pi fc\ t) \quad (3)$$

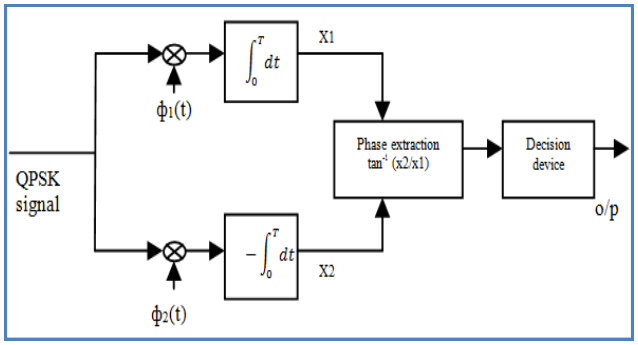

Fig. 1- Demodulation process of BM-QPSK

The outputs of the multipliers are fed to the integrators which integrate the signal in the interval (0, T) (correlation process) and produce the mean x1 and x2 as shown in the [Fig-1]. Further these mean values x1 and x2 are fed to the phase extraction block which computes the inverse tangent of x2/x1 and gives the phase angles associated with the dibits. After the phase is extracted it is then fed to the decision device which compares the extracted phase value against the predefined threshold and decision is made to recover the transmitted data [8].

Implementation of IQ channel Quadrature Phase Shift Keying

For both Balanced modulation QPSK explained in section II and the IQ channel QPSK, the MATLAB implementation is done given a carrier frequency of 500 kHz and data rate of 1Mbps. In order to have 1Mbps data rate 500 kilo symbols per second baud rate is required, because in QPSK two bits are sent per symbol. As the data rate is 1Mbps, the bit period comes out to be 0.1µs and symbol period would be 0.2µs (two bits per symbol). Therefore the number of samples per symbol is found to 100 when it is computed using the above communication parameters. Meaning each QPSK symbol would have 100 samples this can be visualized as one frame which is essential for the frame synchronization explained in the next section.

The binary data stream is split into the in-phase and Quadrature-phase components. These are then separately modulated onto two orthogonal basis functions. In this implementation, two sinusoids are used. Then, the two signals are superimposed, and the resulting signal is the Coherent QPSK signal.

We use the polar non-return-to-zero encoding. These encoders can be placed before for binary data source, but have been placed after to illustrate the conceptual difference between digital and analog signals involved with digital modulation [8].

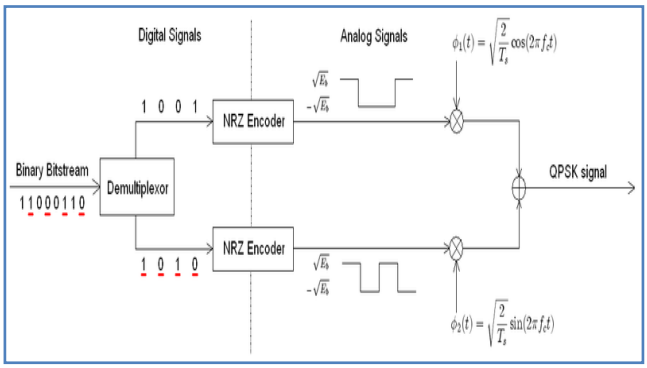

Fig. 2- Coherent QPSK transmitter

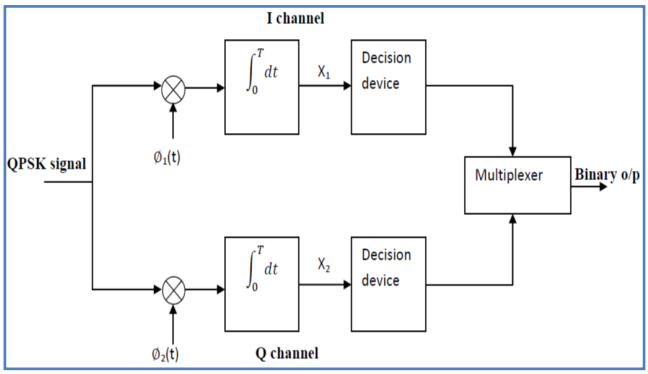

Fig. 3- Coherent QPSK Receiver

For an Additive Whit Gaussian Noise channel, when the transmitted signals are equally likely, the optimum receiver which minimizes average probability of error is a correlation receiver [Fig-3]. The Coherent QPSK Receiver consists of a pair of correlators (multiplier and integrator) with locally generated pair of coherent reference signals ϕ_1 (t) and ϕ_2 (t). The QPSK signal is passed through these two correlators to get x1 and x2. In conventional QPSK receiver a decision is made by comparing x1 and x2 with threshold of zero volts. But in the proposed QPSK receiver the symbol energy E is taken as the reference threshold, i.e., if voltage x1 or x2 is near to +E then decision is made in favor of symbol 1; likewise if voltage x1 or x2 is near to -E then decision is made in favor of symbol 0. This is done because the QPSK modulated signal undergoes lots of degradation when travelled through the communication channel and amplitude would have changed drastically due to various noise effect and hence keeping the threshold as zero would serve for wrong decision of transmitted data bits. The output of both channels is multiplexed to get binary output.

Proposed Frame Synchronization Algorithm

Frame synchronization is the process in the telecommunications transmission system to align the digital channel (time slot) at the receiving end with the corresponding time slot at the transmission end as it occurs. Frame Synchronization techniques are used in order to ensure that signals transmitted from one participant of the communication can be correctly decoded by the receiver.

Before feeding the QPSK signal in to the receiver the frame has to be synchronized. In the proposed system the QPSK modulated signal is divided in terms of frames, each frame contains 100 samples of a symbol which corresponds to 2 input data bit (dibits). This frame sequence when received at the receiver may contain starting

frame being corrupted or some samples missing. In this case the demodulator erroneously considers the wrong samples and decodes the wrong bits, there for there is a need to find the offset or the starting point of the new frame and discard the samples of the corrupted frame.

The main aim of the proposed frame synchronization algorithm is to find the offset (starting point) position of the new frame in the received signal. By knowing the offset point the samples of the previous frame or the corrupted frame is simply discarded and the remaining frames are demodulated and thereby recovering the correct data bits.

The proposed frame synchronization algorithm include the following steps

Step1: Take the first 100 samples of the received signal in an array, say x.

Step2: Now compute

$$A1 = x(n) * (\cos(2\pi\, fc\, n\, ts) + \sin(2\pi\, fc\, n\, ts)) \text{ Where n= 1, 2..100.}$$

Step 3: If A1 = { a_1 , a_2 , a_3 , a_4 ..... a_{100} } compute B1 = {a1, (a_1+ a_2), (a1+a_2+a_3),..., (a_1+a_2+.... +a_{100})}.

Step4: Now compute

$$A2 = x(n) * (\cos(2\pi\, fc\, n\, ts) - \sin(2\pi\, fc\, n\, ts)) \text{ where n=1, 2, 3, 4..100.}$$

Step 5: Repeat the step 3 for A2 to compute the array B2.

Step 6: Find and compare the variance of arrays B1 and B2.

Step 7: The Array with the maximum variance is chosen and passed through LPF to remove unwanted frequencies .

Step 8: Now if the filtered output F = { f_1, f_2 , f_3, f_4,..... f_{100}}, then Compute O= { (f_2-f_1), (f_3-f_1), (f_4-f_1),.....,(f_{100}-f_1)}.

Step 9: Determine the positions of the maximum and the minimum value in the array O.

Step 10: The position which is nearest to the extremities 0 or 100 is the OFFSET (starting point) of the received signal.

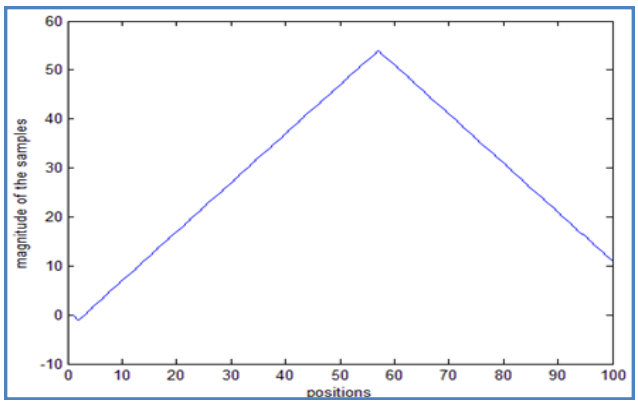

Fig. 4- Output at the End of Step 10 in the Proposed Frame Synchronization Algorithm

[Fig-4] shows the output of the frame synchronization algorithm when executed on Matlab, it can be observed that the maximum and the minimum value occurs at the positions 55 and 2 respectively, hence 2 is chosen as the offset because 2 is nearest to 0 than 55 near to 100.

Implementation on TMS320C6713 DSK

Modulation and demodulation were checked in real time environment using TI's TMS320C6713 DSP Starter Kit, whose salient features include AIC23 stereo codec (ADC and DAC), 4 LEDs and 4 DIP switches as a simple way to provide the user with interactive feedback, 32-bit EMIF for the SDRAM (CE0) and daughter card expansion interface (CE2 and CE3), 8-96 kHz sample rates, 16 MB dynamic RAM, 512kB FLASH memory and USB interface to PC. A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. An included 5V external power supply is used to power the board.

The C6713 DSK is communicated through the Code Composer Studio V3.1 and has been programmed with the optimized code which involves the use of PING-PONG buffer.

The AWGN is added to the system by the use of 4 DIP switches. The 4 DIP switches can be pressed totally in 16 different ways; each combination of the 4 switches is assigned a particular value which is generated when the corresponding combination of the switch is pressed. The DSP Starter Kit makes use of this key value and generates the corresponding level of noise. Hence this noise is used to corrupt the QPSK signal. A total of 16 levels of noise can be added to the system in real-time to corrupt the QPSK signal [9].

Results and Discussion

The results presented here is for 10 Kbits of data. The QPSK modulated wave is passed through Additive White Gaussian Noise (AWGN) channel with different E_b/N_0 values and the corresponding theoretical and practical Bit Error Rates (BER) are calculated.

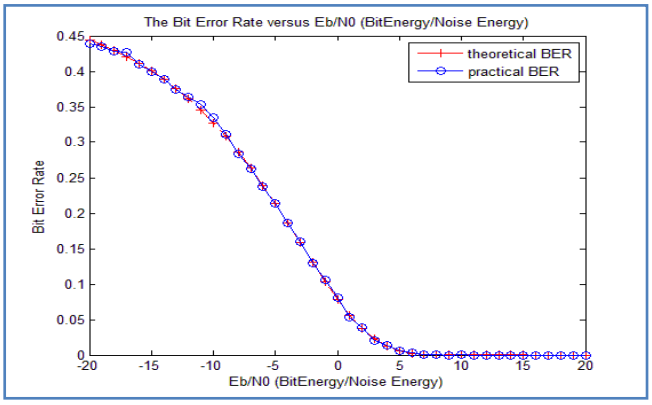

Fig. 5- BER versus E_b/N_0 for BM method

[Fig-5] shows the plot of BER versus E_b/N_0 for the BM-QPSK system, the theoretical and practical values are very close to each other and it is found that the mean of the difference between the theoretical and practical BER values is 0.0023, variance and the Standard Deviation of the difference between the theoretical and practical BER is found to be 8.120×10^{-6} and 0.0028 respectively.

[Fig-6] Showing the plot of BER versus E_b/N_0 for the IQ-QPSK system, here the mean, variance and the standard deviation is found to be 0.0022, 9.413×10^{-6} and 0.0031 respectively.

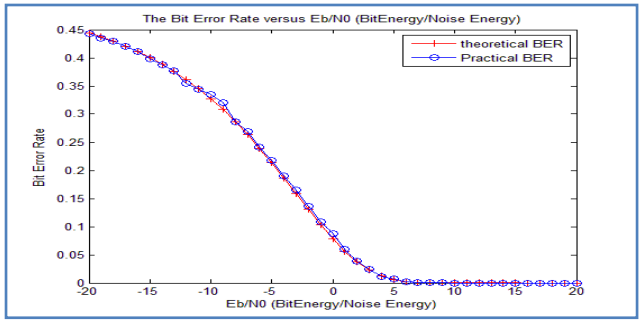

Fig. 6- BER versus E_b/N_0 for IQ channel method

[Fig-7], [Fig-8], [Fig-9] and [Fig-10] demonstrate the result obtained on the TMS320C6713 DSK.

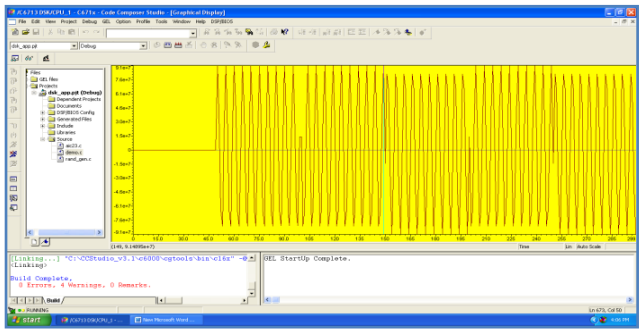

Fig. 7- QPSK wave without noise

[Fig-7] shows the QPSK waves when none of the DIP switches in the C6713 DSK are pressed, i.e. when no noise is added.

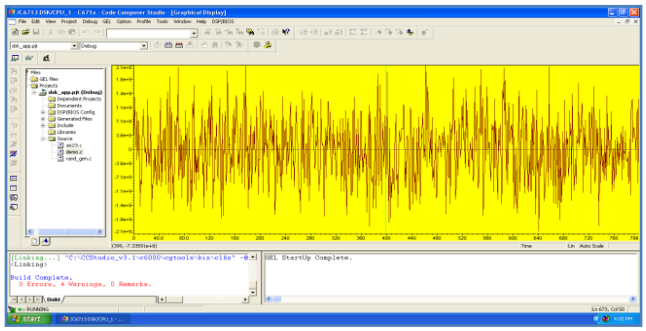

Fig. 8- QPSK wave with noise

[Fig-8] shows the effect of noise on the QPSK wave when the DIP switches value is 12.

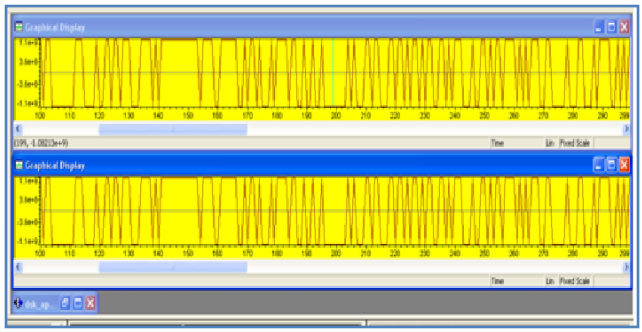

Fig. 9- Recovered data

The recovered data signal is shown in [Fig-9]. The top part of the figure shows the original input data that was used to modulate the carrier and down part shows the recovered data from the QPSK signal when E_b/N_0 = 10 db.

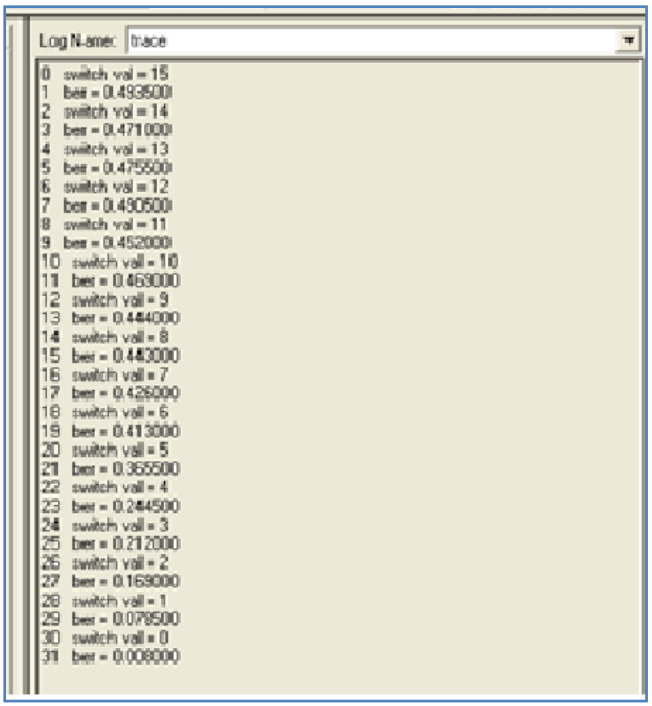

Fig. 10- BER results for various levels of noise

When all the 16 levels of noise are given sequentially to the system it computes the practical BER in real time and displays the output as shown in the [Fig-10].

Conclusion

The proposed QPSK communication system was implemented on Matlab, C programming and on TMS320C6713 DSK. In each case theoretical and practical BER was computed. The comparison between the both is shown in the [Table-2].

Table 2- Comparison of IQ and BM Method

QPSK type	Mean of the difference between the theoretical and practical BER values	Standard deviation between theoretical and practical values
IQ method	0.0022	0.0031
BM method	0.0023	0.0028

The proposed communication system does not compromise either power or bandwidth since QPSK was used as the modulation scheme and has been implemented on the power efficient C6713 DSP Processor. Here the co-relation receiver was used for recovering the data bits, hence the carrier and phase was automatically synchronized at the receiver therefore only frame synchronization was implemented in the proposed model. Further matched filter receiver can be used in place of co-relation receiver and there by PLL (Phase Locked Loop) and symbol timing recovery systems can be implemented as a future enhancement.

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