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VLSI AND FABRICATION

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Abstract- Since the invention of the integrated circuit in 1988,the number of processing steps required to make one has grown from Less than 10 to several hundreds. At the same time-, the silicon wafers on which the VLSI ICs. are produced have gone from being coin sized to being dinner-plate sized. Today one of these 300-mm wafers can yield more than 700 ICs. With such a large number of les coming from a single wafer and with wafers coming off manufacturing lines at rates of tens or thousands a month* companies can quickly find themselves suffering from 1oosses especially in turbulent markets .Batch process which is being followed nowadays by VLSI chip makers is one of the main reasons for these losses. In batch process machines work on a large batch of wafers at the same time and take more than three months to produce VLSI ICs. To avoid the over production of chips, one method is to go for single wafer process. In single wafer process semiconductor companies will be able to produce chips more quickly when the orders came in in the exact quantities specified by those orders. In this paper the IC- fabrication steps are given in brief. Batch process and the Single wafer process are compared in detai1. In the following years all manufacturers will inevitably adopt single Wafer manufacturing process in order to have fast and cheaper, smaller and good quality chips.
Key words- VLSI ICs, VLSI chip makers, IC- fabrication, Wafer manufacturing, semiconductor

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Introduction

Very-large-scale integration (VLSI) is the process of creating integrated circuit by combining thousands of transistor into a single chip. VLSI began in the 1970s when component semiconductor and communication technologies were being developed. The microprocessor is a VLSI device.

The first semiconductor chips held two transistors each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as small-scale integration (SSI), improvements in technique led to devices with hundreds of logic gates, known as medium-scale integration (MSI). Further improvements led to large scale integration 9(LSI). systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessor have many millions of gates and billions of individual transistors.

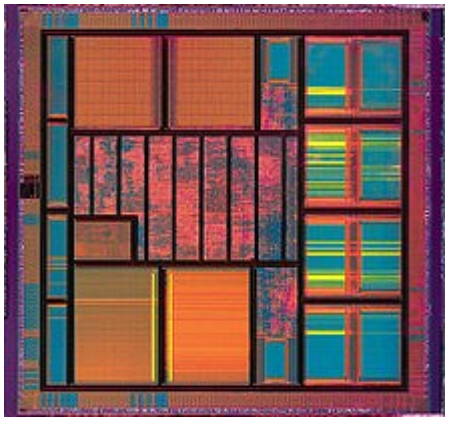

Fig. 1- IC circuit

At one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like Ultra large scale integration But the huge number of gates and transistors available on common devices has rendered such fine distinctions moot. Terms suggesting greater than VLSI levels of integration are no longer in widespread use. As of early 2008, billion-transistor processors are commercially available. This is expected to become more commonplace as semiconductor fabrication moves from the current generation of 65nm processes to the next45nm generations (while experiencing new challenges such as increased variation across process. A notable example is Nvidia's 280 s. series GPU

History & Evolution

The development of microelectronics spans a time which is even lesser than the average life expectancy of a human, and yet it has seen as many as four generations. Early 60's saw the low density fabrication processes classified under Small Scale Integration (SSI) in which transistor count was limited to about 10. This rapidly gave way to Medium Scale Integration in the late 60's when around 100 transistors could be placed on a single chip. Transistor -Transistor logic (TTL) offering higher integration densities outlasted other IC families like ECL and became the basis of the first integrated circuit. By mid eighties, the transistor count on a single chip had already exceeded 1000 and hence came the age of Very Large Scale Integration or VLSI. The second age of Integrated Circuits revolution started with the introduction of the first microprocessor, the 4004 by Intel in 1972 and the 8080 in 1974.

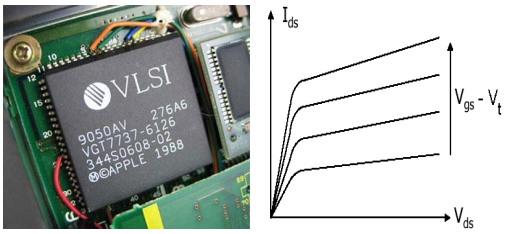

Fig. 2- MOS transistor

Voltage on gate controls current that flows between source and drain. Vt - is the threshold voltage on the gate when drain current begins to flow. To make the channel conductive Vgs has to be greater than Vt. To make the current flow Vdrain has to be greater than Vsource. Here is how transistor looks on layout Drain and source are usually of green or yellow color, gate is red. Transistor is formed when poly (red color) crosses diffusion layer. W and L are geometry parameters,that actually define the technology. L - defines MAX current, because the larger L the lower R (electrical impedance). From the other side, large W - means large Capacitance (C=EWL/d). apacitance is also increasing with higher integration.

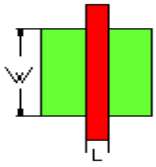

Fig. 3-

VLSI Technology PMOS technology based on P-MOS transistors was invented first. NMOS technology based on n-MOS transistors was used later. n-MOS transistors have better onductance, smaller size and better speed/square performance. CMOS technology combines n-MOS and p-MOS and has greatest power consumption parameters. This image illustrates a cross section of CMOS inverter.

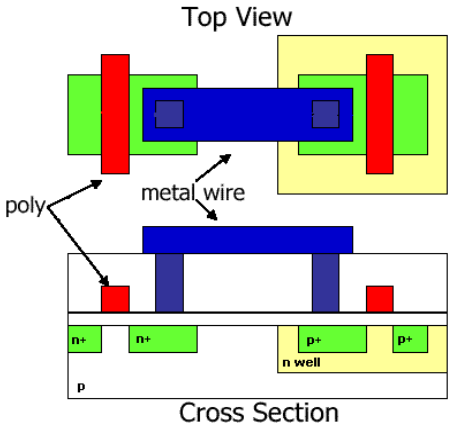

Fig. 4-

VLSI Fabrication

A typical submicron CMOS process uses p-type wafers. A blank 8-inch wafer costs about $100. An IC fabrication process contains a series of masking steps to create layers that define the transistors and metal interconnect. Most layers are formed by the following steps: put layer, protect needed area with photoresist, apply light to transpose, remove photoresist and unprotected layer areas. This photolithografy process is illustrated on the image n-well and p-well are formed by ion implantation, when ions of dopped silicon n+ or p+ are forced into wafer area with a great speed. During the implantation the ions can get inside to a depth of a few microns. Further transistor layers are formed by diffusion (high T ion migration). Gates are created from poly (polycristalline silicon). Poly has to have a good conductance. To improve the coductance poly is covered with a silicide (a metallic compaund of silicon). SIO2 is an insulator, it also protects the outer layer from oxidation. Layers of poly and SiO2 can be deposited using chemical vapor deposition (CVD). Metal layers can be deposited using sputtering.All these layers are patterned using masks and hotolithografy process.

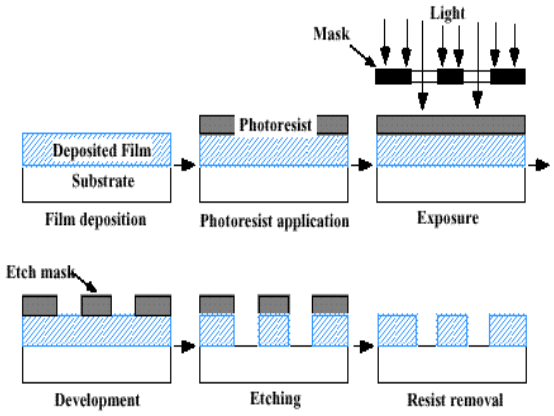

Fig. 5-

Power Consumption

Static power consumption is defined by leakage. Leakage is a junction currents caused by thermally generated carriers. Their

value increases exponentially with increasing junction T. For example, 85C (a common junction T) results in increase by a factor of 60 over room T. Dynamic power consumption depends on a capacitive load W= CV2 (charging C to Vdd draws CV2 energy from power supply). This energy is consumed for every 1 -> 0 and 0 -> 1 transition. Therefor, the higher clock frequency the higher power consumption (~f). The alternative - is to lower V (power supply voltage). 2.3 The CMOS n-Well Process Having examined the basic process steps for pattern transfer through lithography, and having gone through the fabrication procedure of a single n-type MOS transistor, we can now return to the generalized fabrication sequence of n-well CMOS integrated circuits, as shown in Fig. 2.1. In the following figures, some of the important process steps involved in the fabrication of a CMOS inverter will be shown by a top view of the lithographic masks and a cross-sectional view of the relevant areas. The n-well CMOS process starts with a moderately doped (with impurity concentration typically less than 1015 cm-3) p-type silicon substrate. Then, an initial oxide layer is grown on the entire surface. The first lithographic mask defines the n-well region. Donor atoms, usually phosphorus, are implanted through this window in the oxide. Once the n-well is created, the active areas of the nMOS and pMOS transistors can be defined.

Dealing with VLSI Circuit

VLSI Digital circuits are predominantly CMOS based. The way normal blocks like latches and gates are implemented is different from what students have seen so far, but the behaviour remains the same. All the miniaturisation involves new things to consider. A lot of thought has to go into actual implementations as well as design. Let us look at some of the factors involved …

1. Circuit Delays- Large complicated circuits running at very high frequencies have one big problem to tackle - the problem of delays in propagation of signals through gates and wires ... even for areas a few micrometers across! The operation speed is so large that as the delays add up, they can actually become comparable to the clock speeds.
2. Power- Another effect of high operation frequencies is increased consumption of power. This has two-fold effect - devices consume batteries faster, and heat dissipation increases. Coupled with the fact that surface areas have decreased, heat poses a major threat to the stability of the circuit itself.
3. Layout- Laying out the circuit components is task common to all branches of electronics. Whats so special in our case is that there are many possible ways to do this; there can be multiple layers of different materials on the same silicon, there can be different arrangements of the smaller parts for the same component and so on. The power dissipation and speed in a circuit present a trade-off; if we try to optimise on one, the other is affected. The choice between the two is determined by the way we chose the layout the circuit components. Layout can also affect the fabrication of VLSI chips, making it either easy or difficult to implement the components on the silicon.

Advantages

- Power usage/Heat dissipation- As threshold voltages have ceased to scale with advancing process technology, dynamic power dissipation has not scaled proportionally. Maintaining logic complexity when scaling the design down only means that the power dissipation per area will go up. This has given rise to techniques such as dynamic voltage and frequency scaling (DVFS) to minimize overall power.
- **Process Variation-** As photolithography techniques tend closer to the fundamental laws of optics, achieving high accuracy in doping concentrations and etched wires is becoming more difficult and prone to errors due to variation. Designers now must simulate across multiple fabrication process corners before a chip is certified ready for production.
- **Stricter Design Rules-** Due to lithography and etch issues with scaling, design rules for layout have become increasingly stringent. Designers must keep ever more of these rules in mind while laying out custom circuits. The overhead for custom design is now reaching a tipping point, with many design houses opting to switch to electronic design automation (EDA) tools to automate their design process.
- **Timing/Design Closure-** As clock frequencies tend to scale up, designers are finding it more difficult to distribute and maintain low clock skew between these high frequency clocks across the entire chip. This has led to a rising interest in multicore and multiprocessor architectures, since an overall speedup can be obtained by lowering the clock frequency and distributing processing.

First-Pass Success- As die sizes shrink (due to scaling), and wafer sizes go up (to lower manufacturing costs), the number of dies per wafer increases, and the complexity of making suitable photomasks goes up rapidly. A mask set for a modern technology can cost several million dollars. This non-recurring expense deters the old iterative philosophy involving several "spin-cycles" to find errors in silicon, and encourages first-pass silicon success. Several design philosophies have been developed to aid this new design flow, including design for manufacturing (DFM), design for test (DFT), and Design for X

Conclusion

VLSI technology is the enabling technology for a whole host of innovative devices and systems that have changed the way we live. Integrated circuits are much smaller and consume less power than the discrete components used to build electronic systems before the 1960s. Integration allows us to build systems with many more transistors, allowing much more computing power to be applied to solving a problem. Integrated circuits are also much easier to design and manufacture and are more reliable than discrete systems; that makes it possible to develop special-purpose systems that are more efficient than general purpose computers for the task at hand.

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